

What is claimed is:

1. A method for forming a semiconductor device having a trench top isolation layer, comprising the steps of:
 3. providing a substrate having at least one trench therein;
 5. forming a collar insulating layer over the sidewall of a lower portion of the trench;
 7. forming a first conductive layer protruding to the collar insulating layer in the lower portion of the trench;
 10. forming a second conductive layer overlying the first conductive layer and covering the collar insulating layer;
 13. forming an insulating spacer over an upper portion of the sidewall of the trench and separated from the second conductive layer by a gap;
 16. thermally oxidizing a portion of the second conductive layer to form an oxide layer thereon whereby the gap is filled;
 19. removing the oxide layer to expose the second conductive layer;
 21. forming a reverse T-shaped insulating layer by chemical vapor deposition to serve as the trench top isolation layer; and
 24. removing the insulating spacer.
1. The method as claimed in claim 1, further forming a gate insulated from the substrate and overlying the reverse T-shaped insulating layer.

1 3. The method as claimed in claim 1, wherein the
2 collar insulating layer is a silicon oxide layer.

1 4. The method as claimed in claim 1, wherein the
2 first conductive layer is a polysilicon layer.

1 5. The method as claimed in claim 1, wherein the
2 second conductive layer is a doped polysilicon layer.

1 6. The method as claimed in claim 1, wherein the
2 insulating spacer is composed of a pad oxide layer and an
3 overlying silicon nitride layer.

1 7. The method as claimed in claim 6, wherein the
2 insulating spacer has a thickness of about 200-300Å.

1 8. The method as claimed in claim 1, wherein the gap
2 has a width of about 50-60Å.

1 9. The method as claimed in claim 1, wherein the
2 reverse T-shaped insulating layer is formed by low pressure
3 chemical vapor deposition (LPCVD).

1 10. The method as claimed in claim 1, wherein the
2 reverse T-shaped insulating layer is a tetraethyl
3 orthosilicate (TEOS) oxide.

1 11. A semiconductor device having a trench top
2 isolation layer, comprising:

3 a substrate having at least one trench formed therein;
4 a collar insulating layer disposed over a lower portion
5 of the sidewall of the trench;

6 a first conductive layer disposed in the lower portion
7 of the trench and protruding the collar
8 insulating layer;
9 a second conductive layer disposed overlying the first
10 conductive layer and covering the collar
11 insulating layer;
12 a reverse T-shaped insulating layer disposed overlying
13 the second conductive layer to serve as the
14 trench top isolation layer; and
15 a gate disposed overlying the reverse T-shaped
16 insulating layer and insulated from the
17 substrate.

1 12. The semiconductor device as claimed in claim 11,
2 wherein the collar insulating layer is a silicon oxide
3 layer.

1 13. The semiconductor device as claimed in claim 11,
2 wherein the first conductive layer is a polysilicon layer.

1 14. The semiconductor device claimed in claim 11,
2 wherein the second conductive layer is a doped polysilicon
3 layer.

1 15. The semiconductor device claimed in claim 11,
2 wherein the reverse T-shaped insulating layer is a
3 tetraethyl orthosilicate (TEOS) oxide.